Hierarchical Design and Analysis Environment

PlanAhead

Improve performance and capacity while reducing design time
Design Complexity Increasing

- More and more FPGA designs are Platform designs today
  - Users integrating more functionality into the FPGA
- Large SoC designs implemented in Platform FPGAs have higher complexity
  - Multiple clock domains common in many designs
  - Hierarchical designs
  - Multiple timing constraints
  - Higher routing density and utilization density
  - Use of multiple hard IP features (BRAM, processor DSP…)

*PlanAhead Helps Solve The Challenges of Today’s Complex Designs*
PlanAhead Key Drivers

What our customers are telling us they want

• Meeting timing budgets is still the #1 goal of designers*
  – Need greater certainty of meeting performance goals and tighter correlation between logic and physical domains
  – Higher performance = lower cost (or more functions)
  – Higher performance = longer field life of the end products

• Most designers willing to adopt new methodologies if it:
  – Achieves better performance
  – Reduces time to design closure
  – Helps in automating design iterations

* 2005 FPGA EDA Survey by CMP
PlanAhead Software
Hierarchical Design and Analysis

- Streamlines the step between Synthesis and Place & Route
  - Analyze timing, connectivity, resource utilization, constraints, etc...
  - Visually analyze & detect design problems early
  - Fix designs w/o having to iterate back
- Flexible Floorplanning
- Enables a Block-based Methodology
- Easy-to-use; Intuitive – Faster timing closure

Performance Above and Beyond ISE 8.1
- Achieve an average of 24% faster performance
- Over 50% better performance for tough, multi-clock designs
The Value of PlanAhead

- **PlanAhead with Virtex-4 FPGAs Delivers Performance where Competing Solutions Cannot**
  - Achieve an average of 30% faster performance
  - Over 57% better performance for tough, multi-clock designs
  - Get a two speed-grade advantage over competing solutions

- **Productivity - Faster Design Closure**
  - Reduce the number of iterations
  - Solve problems physically – not in RTL

- **Results Repeatability**
  - Increase implementation consistency
  - Create and reuse IP modules

*Up to Two Speed grades faster with PlanAhead Software and Virtex-4 FPGAs vs. Competing Solutions*
Who Should Use PlanAhead?

• **Challenging Designs**
  – Large devices, complex constraints, heavy utilization
  – Advantages seen with devices as small as Virtex-4 LX15

• **Users Experiencing Implementation Issues**
  – Performance, Capacity, Runtime, Repeatability

• **Users Wanting More Insight into their Designs and Implementation Control**
  – Users not adverse to interactive tools and methodology

• **Users Wanting a Block-based Design Methodology**
  – Module-level Incremental updates
  – Provides an IP reuse solution
What are the PlanAhead Benefits?

and...

How does PlanAhead differ from ISE Tools such as Floorplanner and PACE?
Quickly Identify Bottlenecks

- Unique Visibility into Design
  - Schematic, Device, Netlist, Timing, Hierarchy, Package
  - Visual metric maps
  - All views Cross-highlight

- Timing Analysis
  - Pre or post ISE implementation
  - Quickly identify problem areas

- Design Rule Checks
  - Find errors early

- Flexible Select/Highlight
  - Easily find, highlight or trace logic
Visualize and Explore Logic

• Schematic Viewer
  – Generate at any logic level
  – Traverse logic hierarchy
• Hierarchy Viewer
  – Locate logic within context of design
• Selectively Expand Logic
  – View any selected logic
  – View all timing path instances
  – Interactively expand logic
  – Identify critical path modules
  – Easily select logic to floorplan

Quickly Identify and Constrain Critical Logic
Explore Implementation Options

• Queue multiple runs with various ISE strategies or constraints
  – Create user defined or use factory shipped Strategies

• Manage Run data and monitor status
  – Easily manage all project run data from GUI
  – Use multiple processors, if available
  – ISE log file viewer

• Project maintains the state of the design
  – Upon opening project, run status is displayed
Timing Analysis

- Prior to ISE Implementation
  - Verify design feasibility
  - Identify RTL issues early
- Robust Analysis Options
  - Calculate timing with or without estimated interconnect delays
- Results Viewer
  - Sort and select critical paths
  - Identify logic to floorplan

Reduce Iterations by Finding Problems Early
Robust Design Rule Checking

- Catch Errors Early with DRCs
  - Robust set of IO, Clock, Floorplan rules
  - Highlights errors and misused resources
- Quickly Identify Problem Areas
  - Selectively highlight placement and timing paths

Visualize and Fix Implementation Issues
Faster Timing Closure

• Analyze Multiple Results from ISE
  – Highlight failing timing paths from post-route timing analysis
  – Quickly identify, select and constrain critical path logic

• Hierarchical Floorplanning
  – Guide place and route toward better results
  – Robust Block creation capabilities

• Utilization Estimates
  – All resource types shown for each Block
  – Clocks, Carry Chains, RPMs, etc…

• Connectivity Display
  – IOs, Net Bundles, Clock Domains

*Customer Proven – Better Performance in Less Time*
Achieve that Last Bit of Design Utilization or Performance

- **Increase Device Capacity**
  - Compress logic within blocks

- **Improve Performance by Floorplanning**
  - Easy and intuitive environment
  - Visualize issues and solve quickly
Reuse Successful Results

• Enable Incremental Updates that Work
  – PlanAhead can update any logic module netlist separately
  – Utilize floorplan for Incremental Guided routing
  – Focuses only on modules that change
  – Preserves performance of surrounding logic

• Export and Reuse IP Modules
  – Export with fixed or relative placement
  – Usable in any device of same family
  – Ensure performance and size targets

*PlanAhead Leverages the Hierarchy*
The PlanAhead Advantage

PlanAhead Performance Advantage Relative To ISE Timing-driven Flow

- Suite of 15 tough customer designs
  - Average logic utilization 78%
  - Average Fmax improvement 24% (30% vs. competition)
  - Over 2 speeds faster than competing solutions

- For the 5 multi-clock designs:
  - Average logic utilization 85%
  - Average Fmax improvement 51% (57% vs. competition)
Summary

• ISE Fmax Technology Delivers Highest Virtex-4 Performance
  – Performance Evaluation: 37% better performance in ISE 8.1i over previous release for unconstrained designs
  – Experienced FPGA Users: 10 - 37% better performance in ISE 8.1i over previous release

• The PlanAhead Advantage for Virtex-4 Performance
  – 30% average performance improvement for Virtex-4 FPGAs using industry-unique PlanAhead tools vs. competing FPGAs
  – Up to two speed grades in cost-savings over competing solutions

Making the World’s Fastest FPGAs Run Faster
More Information

• Give your fastest Virtex-4 FPGAs a performance boost

• To try a 60-day evaluation of ISE 8.1i Fmax technology or buy, visit www.xilinx.com/ise

• To learn more, visit the PlanAhead Web site www.xilinx.com/planahead
  – Download a free 30-day PlanAhead evaluation
    • Contains a detailed interactive tutorial
  – Watch a PlanAhead demonstration video

*Take a Test Drive. You’ll Love the Speed!*
Additional Presentation Slides
Virtex-4 Case Study
Design #15

- Virtex-4 FX60 device, 3 clocks
  - Utilization:
    88% logic
    58% Block RAM
    28% DSP
- Inconsistent place-and-route results & performance not met
- Shares common critical logic with four other Virtex-4 designs
- Did 4 floorplan iterations and achieved:
  - Performance increased 102% and timing goals met
    - Clocks before: 92 MHz, 77 MHz, 66.67 MHz
    - Clocks after: 200 MHz, 156 MHz, 125 MHz
  - Runtimes dropped from ~24 hrs to 80 min
  - Able to use floor plan for critical logic in 4 related designs
Virtex-4 Case Study
Design #13

- Xilinx reference design for ML410 development board
- 40% logic utilization in Virtex-4 FX60, 4 clocks
- Goal: Compact logic around PowerPC and guarantee performance
- 2 days of floor planning with PlanAhead resulted in:
  - 39% performance improvement
    - Clocks before: 64 MHz, 266 MHz, 67 MHz, 121 MHz
    - Clocks after: 100 MHz, 340 MHz, 101 MHz, 146 MHz
  - Runtime reduction from 9.6 hours to 2.6 hours

![Graph showing performance improvements](chart.png)
Virtex-4 Case Study #13 Results

- Tight, highly utilized floorplan around PowerPC
  - Floorplan available to ML410 users so processor logic performance remains consistent
PlanAhead Development Plans

• Continue to Develop as Separate Tool
  – Remain targeted as high-end design solution outside of ISE
  – Long Range plans to develop some capabilities in ISE
  – Technology ~2 Years Ahead of ISE Floorplanner and PACE

• Maintain Fast Development Pace
  – Continue to introduce leading edge technology
  – Able to react quickly to customer issues and requests
  – 9 dedicated development engineers
  – 3-4 Major releases per year

Customer Support Focused with Rapid Response!
Need a PlanAhead QuickStart?

- **Expert Assistance for Design Issue Resolve or Knowledge Transfer**
  - 5 days of on-site assistance by a trained Xilinix Engineer
  - Project scope driven by customer requirements
    - Setup & customization of PlanAhead software
    - Utilize PlanAhead to achieve design improvements or issue resolve
    - Assess the skills and needs of the customer’s team
    - Develop rollout plan to ensure the team has the knowledge to reduce risk and complete the project on schedule
    - Deliver 2-Day training course at the customer site
How Does PlanAhead Compare with Altera Quartus II Software

• Entirely Different Tool Methodology
  – Quartus II tries to simplify the flow
  – Tries to make it all a push-button approach
  – Takes implementation control away from the user
  – What happens when that doesn’t work?

• Few Usable Interactive Capabilities
  – Logic Lock cumbersome and rarely used
  – Often cause problems in Fitter stage with vague messages
  – Weak block-based capabilities

• Problematic When Tried “PlanAhead-style”