Reiner Hartenstein

(for speaker introduction)

http://hartenstein.de

Dr.-Ing. Reiner Hartenstein is CS professor (emeritus) at TU Kaiserslautern and adjunct professor at KIT Karlsruhe, as well as consultant, authorized expert and referee on Information Technology.

He was associate professor at Karlsruhe Institute of Technology (KIT), where he had received all academic degrees from the EE department, as a scholar of Karl Steinbuch, founder of the German “Informatik” discipline.

He was visiting professor at UC Berkeley for about half a year in the 80ies.

Reiner Hartenstein is IEEE life fellow, SDPS fellow, FPL fellow. and recipient of several other awards.

He is credited to be the father of High Performance Reconfigurable Computing and, as creator of the **Xputer** paradigm (the counterpart of the von-Neumann-**Computer** paradigm), the initiator of the **twin paradigm** approach to boost HPRC acceleration and productivity. His group at Kaiserslautern developed and implemented Xputer machine principles and a high level programming language. His DPLA accelerator achieved a speed-up factor of 15000, two decades earlier than similar speed-ups obtained by FPGA use.

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He is author and the first implementer of the hardware description language **KARL**, the ground-breaking forerunner of the much less efficient languages like VHDL or Verilog, as well as the backbone of the world’s first CAD framework for VLSI microchip design & test, successful in designing commercially manufactured VLSI microchips.

He is the founder of the German Multi University **"E.I.S." Project**, Germany’s contribution to the Mead-&-Conway VLSI design revolution.

He is the founder of three, and, co-founder of two more international conference series still running successfully.

He co-edited 16 books, wrote 2 books and almost 800 technical papers and gave more than 200 invited talks and 53 keynote addresses as well as 36 invited VLSI design courses, each one covering 3 or 5 full days.