Reiner Hartenstein, Informatik Department,
University of Kaiserslautern, Germany
http://hartenstein.de

reiner@hartenstein.de

Enabling Technologies for Reconfigurable Computing
November 21, 2001, Tampere, Finland

Reiner Hartenstein

University of Kaiserslautern

Enabling Technologies for Reconfigurable Computing

Part 4:
FPGAs: recent developments

Wednesday, November 21, 16.00 - 17.30 hrs.

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Schedule

time	slot
08.30 - 10.00	Reconfigurable Computing (RC)
10.00 - 10.30	coffee break
10.30 - 12.00	Compilation Techniques for RC
12.00 - 14.00	lunch break
14.00 - 15.30	Resources for Stream-based RC
15.30 - 16.00	coffee break
16.00 - 17.30	FPGAs: recent developments

Opportunities by new patent laws ?

- to clever guys being keen on patents:
- don't file for patent following details !
- everything shown in this presentation has been published years ago

>> Fine Grain Reconfigurable Circuits

Fine Grain Reconfigurable Circuits

- Embedded Systems (Co-Design)
- Hardwired IP Cores on Board
- Run-Time Reconfiguration (RTR)
- Rapid Prototyping & ASIC Emulation
- Testing FPGA-based Systems
- Evolvable Hardware (EH)
- Academic Expertise

>> FPGAs: recent developments

http://www.uni-kl.de

- Reconfigurable Computing (RC)
- Compilation Techniques for RC
- Resources for Stream-based RC
- FPGAs: recent developments

Workshop on Enabling Technologies for System-on-Chip Development, November 19-20, 2001, Tampere, Finland
http://www.cs.tut.fi/soc/

Reconfigurable Computing Architectures and Methodologies for System-on-Chip;
Reiner Hartenstein, Monday, November 19, 10:15 - 11:00 hrs.

Configware market

FPGA market

Fine Grain Reconfigurable Circuits

- FPGA Vendors stepping forward
  - Xilinx
    - Software by Xilinx
    - Configware (soft IP Cores)
    - Hardware
  - Altera
    - Software
    - Configware
    - Hardware

Changing Design Flow

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RTR

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ASIC em

ASIC emulation: a new business model ?

- ASIC emulation / Rapid Prototyping: to replace simulation
- Quickturn (Cadence), IKOS (Synopsys), Celaro (Mentor)
- From rack to board to chip (from other vendors, e. g. Virtex and VirtexE family (emulate up to 3 million gates)
- Easy configuration using SmartMedia FLASH cards
- ASIC emulators will become obsolete within years
- By RTR: in-circuit execution debigging instead of emulation

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EH

EH, EM, ...

- "Evolvable Hardware" (EH), "Evolutionary Methods" (EM), „digital DANN", "Darwinistic Methods", and biologically inspired electronic systems
- new research area, which also is a new application area of FPGAs
- revival of cybernetics or bionics: resurrection stimulated by the new technology
- „evolutionary" and the „DNA" metaphor create widely spread awareness
- EM sucks, also thru mushrooming funds in the EU, in Japan, Korea, and the USA
- EM-related international conference series are in their stormy visionary phase, like EH, ICES, EuroGP, GP, CEC, GECCO, EvoWorkshops, MAPLD, ICGA
- Shake-out phenomena expected, like in the past with „Artificial Intelligence"
- should be considered as a specialized EDA scene, focusing on theoretical issues.
- Genetic algorithms suck - often replacable by more efficient ones from EDA
- It is recommendable to set-up an interwoven competence in both scenes, EM scene and the highly commercialized EDA scene
- EH should be done by EDA people, rather than EM freaks.

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Unis

BRASS

- **UC Berkeley,** the BRASS group: Prof. Dr. John Wawrzynek
- Garp integrates processor and FPGA; dev. in parallel w. compiler - software compile techniques (VLIW SW pipelining): simple pipelining schema f. broad class of loops.
- SCORE, a stream-based computation model - a unifying computational model. Fast Mapping for Datapaths: by a tree-parsing compiler tool for datapath module mapping
- HSRA. new FPGA (& related tools) supports pipelining, w. retiming capable CLB architecture, implemented in a 0.4um DRAM process supporting 250MHz operation
- The Pleiades Project, Prof. Jan Rabaey, ultra-low power high-performance multimedia computing through the reconfiguration of heterogeneous system modules, reducing energy by overhead elimination, programmability at just the right granularity, parallelism, pipelining, and dynamic voltage scaling.
- OOCG. Object Oriented Circuit-Generators in Java
- MESCAL (GSRC), the goal is: to provide a programmer's model and software development environment for efficient implementation of an interesting set of applications onto a family of fully-programmable architectures/microarchitectures.

Berkeley claiming

- SCORE, a stream-based computation model: the BRASS group claims having solved the problem of primary impediment to wide-spread reconfigurable computing, by a unifying computational model.
- Remark: a clean stream-based model introduced around 1980: the Systolic Array
- In 1995 a reconfigurable stream-based model introduced by Rainer Kress.
- Fast Mapping for Datapaths (SCORE): BRASS claims having introduced 1998 the first tree-parsing compiler tool for datapath module mapping ." Further, it is the first work to integrate simultaneous placement with module mapping in a way that preserves linear time complexity."
- Remark: The DPSS (Data Path Synthesis System) using tree covering simultanous datapath placement and routing has been published in 1995 by Rainer Kress
- Chip-in-a-Day Project. Prof. Dr. Bob Broderson's „radical rethink of the ASIC design flow aimed at shortening design time, relying on stream-based DPU arrays."
- Remark: the KressArray, a scalable rDPU array [1995] is stream-based

Berkeley: Chip-in-a-Day

- Chip-in-a-Day Project. Prof. Dr. Bob Broderson, BWRD: targeting a radical rethink of the ASIC design flow aimed at shortening design time. Relying on stream-based DPU arrays (not rDPU and related EDA tools. Davis: „... 50x decrease in power requ. over typical TI C64X design
- New design flow to break up the highly iterative EDA process, allowing designers to spend more time defining the device and far less time implementing it in silicon. „... developers to start by creating data flow graphs rather than C code„
- It is stream-based computing by DPU array
- For hardwired and reconfigurable DPU array and rDPU array

Stanford thru BYU

- **Stanford:** Prof. Flynn went emeritus, Oskar Menzer moved to Bell Labs.
- no activities other than YAFA (yet another FPGA application), which
- **UCLA:** Prof. Jason Cong well-known expert on FPGA architectures andR and P algorithms. 9 projects, umtiple sponsors under the California MICRO Program.
- Prof. Majid Sarrafzadeh directs the SPS project: "versatile IPs.., a new routing architecture, architecture-aware CAD, IP-aware SPS compiler
- **USC:** Prof. Viktor Prasanna (EE dept.) works 20% on reconfigurable computing: MAARC project, DRIVE project and Efficient Self-Reconfiguration. -
- Prof. M.Dubois: RPM Project, FPGA-based emuation of scalable multiprocessors.
- DEFACTO proj.: compilation - architecture-independent at all levels
- **MIT.** all MATRIX web pages removed 1999. The RAW project a conglomerate
- **VT.** Prof. P.Athanas: Jbits API for internet RTR logic ($2.7 mio DARPA grant). With Prof. Brad Hutchings, BYU on programming approaches for RTR Systems
- **BYU.** Prof. Brad Hutchings works on the JHDL (JAVA Hardware Description Language) and compilation of JHDL sources into FPGAs.

Toronto thru Karlsruhe

- **U. Toronto.** Prof. J.Rose, expert in FPGA architectures and R & P algorithms.
- The group has developed the Transmogrifier C, a C compiler creating a netlist usable for Xilinx XC4000 and Altera's Flex 8000 and Flex 10000 series FPGAs.
- Founder of Right Track CAD Corporation (PLD CAD), acquired by Altera in 1999
- Los Alamos National Laboratory, Los Alamos, New Mexico (Jeff Arnold) - Project Streams-C: programming FPGAs from C sources.
- Katholic University of Leuven, and IMEC: Prof. Rudy Lauwereins, methods for implementing MPEG-4 like multimedia applications on dynamically reconfigurable platforms, as well as on reconfigurable instruction set processors.
- University of Karlsruhe. Prof. Dr.-Ing. Juergen Becker: hardware/software co-design, reconfigurable architectures and corresponding synthesis techniques, and, technologies for future mobile communication systems.
- Prof. Becker recently worked on design and implementation of dynamically reconfigurable architectures for mobile communication, distributed internet-based CAD methods, partitioning co-compilers for embedded reconfigurable systems.

.... Stream Processors - MSP-3

- 3rd Workshop on Media and Stream Processors (MSP-3)
  - http://www.pdcl.eng.wayne.edu/msp01
- in conj. w. 34th International Symposium on Microarchitecture (MICRO-34)
  - http://www.microarch.org/micro34
- Austin, Texas, December 1-2, 2001
- Topics of interest include, but are not limited to:
  - Hardware/Compiler techniques for improving memory performance of media and stream-based processing
  - Application-specific hardware architectures for graphics, video, audio, communications, and other media and streaming applications
  - System-on-a-chip architectures for media and stream processors
  - Hardware/Software Co-Design of media and stream processors
  - and others ....
- DEADLINES:
  - Paper submission: September 24, 2001
  - Author Notification: October 22, 2001
  - Camera-Ready Papers: November 10, 2001

>> Coarse Grain Reconfigurable Circuits (Reconfigurable Computing)

- Fine Grain Reconfigurable Circuits
- Coarse Grain Reconfigurable Circuits (Reconfigurable Computing)

>> Coarse Grain Reconfigurable Circuits

Coarse Grain Reconfigurable Circuits

- Distributed Computing (DPU arrays
- Different Routes to DPU Arrays
- The Memory Communication Gap
- Reconfigurable Computing (RC)
- Machine Principles for RC
- Compilation Techniques for RC
- Soft CPUs and Arrays
- The FPGA CPU
- Reconfigurable Soft Arrays

>> Distributed Computing (DPU array)

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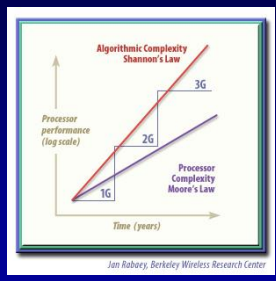
Shannon's Law



- In a number of application areas throughput requirements are growing faster than Moore's law
- Fundamental flaws in software processor solutions
- 32 soft ARM cores fit onto contemporary FPGA
- Stream-based distributed processing is the way to go

Different Routes to DPU Arrays

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EDA for DPU arrays or rDPU arrays

- Several fundamentally different approaches, The first uses fixed DPUs, all other use of reconfigurable DPU arrays
- First application-specific DPU arrays. Fabrication is the last station of the flow, profitable only by very high production volume like for a mass market
- Second, a fully universal coarse grain reconfigurable array using universal
- rDPUs (not very realistic, since area-inefficient, except multi granular approach)
- Third, domain-specific rDPU architecture (Chameleon Systems and PACT Corp.) (design space explorer .... within a day)
- Fourth, soft rDPU array mapped onto a large FPGA: highest flexilbility.
- Clock slower by factor 3: compensated by a higher degree of parallelism
- All four routes have mainly the same design flow front end
- The tendency goes toward stream-based DPU arrays and there is
- No principle difference, whether the DPU array is hardwired or reconfigurable.
- toward FPGA-based "chip-in-one-hour?

The Memory Communication Gap

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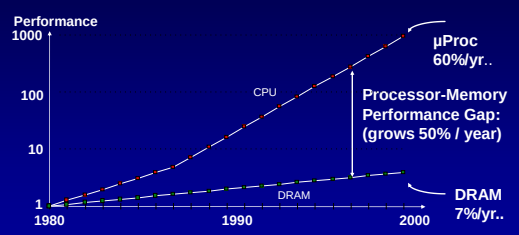
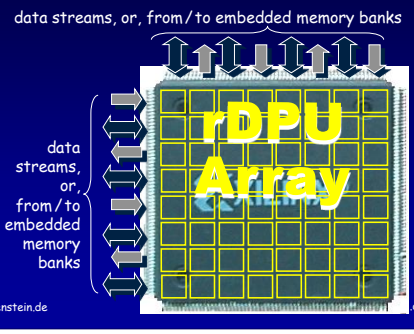
Processor Memory Performance Gap



Array I/O examples



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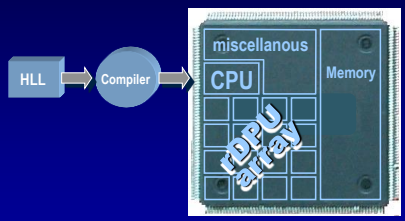

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Machine Principles for RC

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Stream-based

- Stream-based ALU arrays or DPU arrays - instead of arrays of CPUs
- DPUs connected to form a pipe network (multiple pipelines)
- DPUs (Data Path Units) without program controllers
- not multiple CPUs.
- Tailored multiple data streams are pumped thru from outside
- That's why these arrays are called
- "stream-based" arrays.
- KressArray: an early stream-based DPU array, being reconfigurable
- No CPU, nothing "central".

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ASICs dead ?

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(When) Will FPGAs Kill ASICs?

Jonathan Rose
Altera
University of Toronto

My Position [Jonathan Rose]

ASICs Are Already Dead

They Just Don't Know It Yet!

Why? [Jonathan Rose]

1. You have to fabricate an ASIC
   - Very hard, getting harder
2. An FPGA is pre-fabricated
   - A standard part
   - immense economic advantages

Making ASICs is Damn Difficult [Jonathan Rose]

- Testing
- Yield
- Cross Talk
- Noise
- Leakage
- Clock Tree Design
- Horrible very deep submicron effects we don't even know about yet

Did I Mention Inventory? [Jonathan Rose]

- ASIC users must predict # parts
  - 2 or 3 months in advance!
- Never guess the Right Amount
  - Make Too Many – You Pay holding costs
  - Make Too Few – Competitor gets the Sale

[Jonathan Rose] FPGAs Give You

- Instant Fabrication
  - Get to Market Fast
  - Fix 'em quick
- Zero NRE Charges
  - Low Risk
  - Low Cost at good volume
- Lower Health Care Costs

PLDs: "Too Pricey & Too Slow?" [Jonathan Rose]

- Custom IC Designer Can Make Logic
  - 20x Faster,
  - 20x Smaller than Programmable

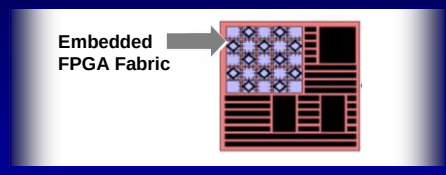
Not So Fast [Jonathan Rose]

- 9 Times Out of 10
  - You make can the thing fast by breaking it into multiple parallel slower pieces
- Result runs just as fast in programmable
  - PLD users do this all the time
  - Good way to spend silicon

One Time out of Ten

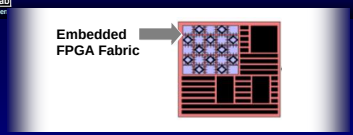
- Need cost & performance of custom core
  - If a good market, we'll put it on our PLDs
- Significant Markets Only
  - ASICs Can Keep the small markets

What About PLD Cores on ASICs?



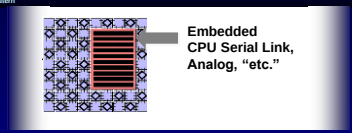
[Jonathan Rose]

What's Wrong with This Picture?



1. Still Have to Make the Chip [Jonathan Rose]
2. Need Two Sets of Software to Build It
   - The ASIC Flow
   - The PLD Flow
3. Have No Idea What to Connect the PLD Pins to
   - Chances Are, You Are Going to Get It Wrong!

What's Right with This Picture!



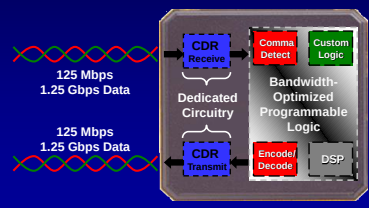
[Jonathan Rose]

1. Pre-Fabricated
2. One CAD Tool Flow!
3. Can Connect Anything to Anything
   - PLDs are built for general connectivity

ASICs Dead - END -

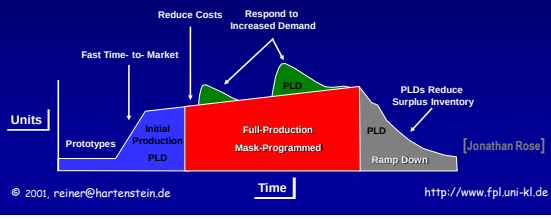
High-Speed Signaling

- PLDs Currently Contain High-Speed Signaling Standards

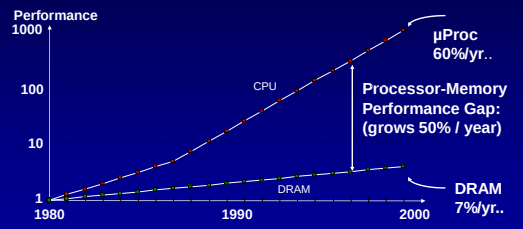


Some Can't Tolerate the Cost Premium

- It's true, high-volume markets demand low cost
- Use PLD at Beginning
- Switch to Mask-Programmed PLD for High Volume
- We Still Do the Fabrication (Don't Worry!)



Processor Memory Performance Gap



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Soft CPU

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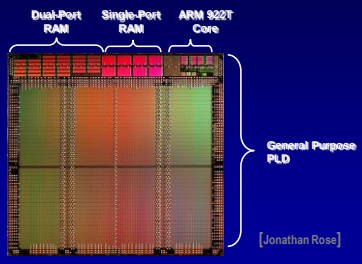
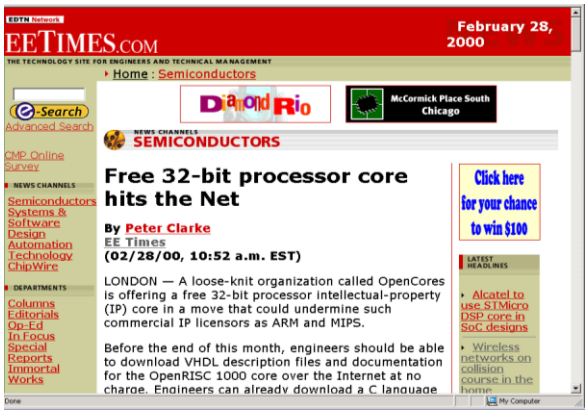
reiner@hartenstein.de

Processors in PLDs: Excalibur

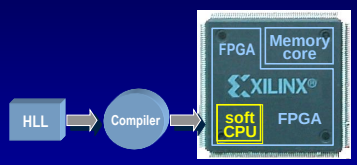
- High-Speed Processors Integrated with PLDs



Available Today!



HLL 2 soft CPU



Some soft CPU core examples

core	architecture	platform
MicroBlaze 125 MHz 70 D-MIPS	32 bit standard RISC 32 reg. by 32 LUT RAM-based reg.	Xilinx up to 100 on one FPGA
Nios	16-bit instr. set	Altera Mercury
Nios 50 MHz	32-bit instr. set	Altera 22 D-MIPS
Nios	8 bit	Altera - Mercury
gr1040	16-bit	
gr1050	32-bit	
My80	i8080A	FLEX10K30 or EPF6016
DSPuva16	16 bit DSP	Spartan-II

core	architecture	platform
Leon 25 Mhz	SPARC	
ARM7 clone	ARM	
uP1232 8-bit	CISC, 32 reg.	200 XC4000E CLBs
REGIS	8 bits Instr. + ext. ROM	2 XILINX 3020 LCA
Reliance-1	12 bit DSP	Lattice 4 isp30256, 4 isp1016
1Popcorn-1	8 bit CISC	Altera, Lattice, Xilinx
Acorn-1		1 Flex 10K20
YARD-1A	16-bit RISC, 2 opd. Instr.	old Xilinx FPGA Board
xr16	RISC integer C	SpartanXL

FPGA CPUs in teaching and academic research

- UCSC: 1990!
- Märaldalen University, Eskilstuna, Sweden
- Chalmers University, Göteborg, Sweden
- Cornell University
- Gray Research
- Georgia Tech
- Hiroshima City University, Japan
- Michigan State
- Universidad de Valladolid, Spain
- Virginia Tech
- Washington University, St. Louis
- New Mexico Tech
- UC Riverside
- Tokai University, Japan

free DSP or Processor Cores

CPU core	Description	Language	Implementation
Reliance 1	12bit DSP and peripherals	Schematic	Viewlogic 7 Lattice CPLDs
PopCorn 1	small 8 bit CISC	Verilog	1 Lattice CPLD isp3256-90
Acorn 1	small 8 bit CISC	VHDL	Max2PlusII+ 1 Altera 10k20
16-bit DSP	A 16-bit Harvard DSP with 5 pipeline stages.	VHDL	Xilinx XC4000
Free-6502	6502 compatible core	VHDL	
DLX	Generic 32-bit RISC CPU	VHDL	Synopsys
DLX2	Generic 32-bit RISC CPU	VHDL	
GL85	i8085 clone	VHDL	
AMD 2901	AMD 2901 4-bit slice	VHDL	
AMD 2910	AMD 2910 bit slice	VHDL	
i8051	8-bit micro-controller	VHDL	Synopsys
i8051	another i8051 clone	VHDL	Mentor Graphics

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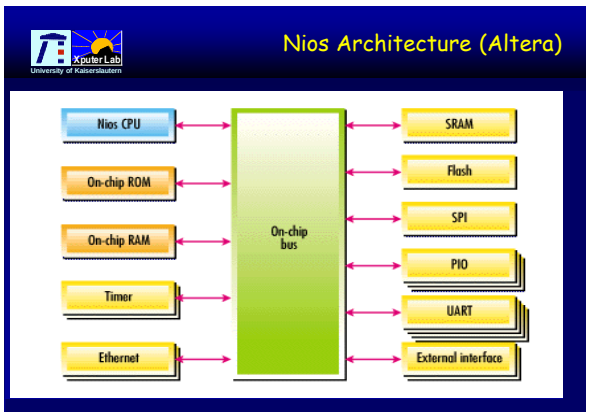


NEWS CHANNELS
SEMICONDUCTORS

Xilinx preps 10 million-gate FPGAs

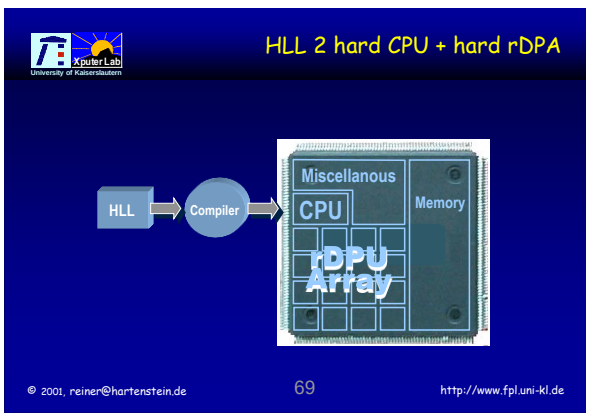
By Craig Matsumoto
EE Times
(05/22/00, 11:38 a.m. EST)

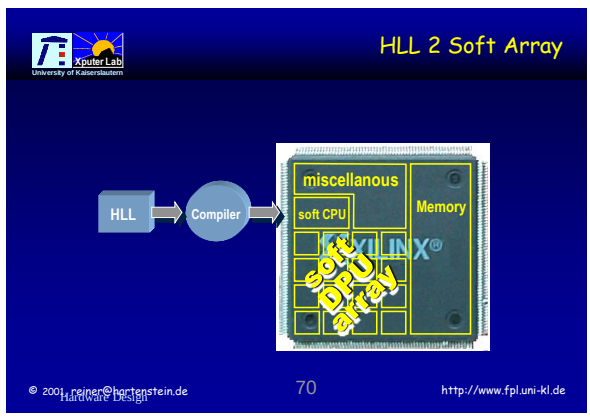
SAN JOSE, Calif. — Xilinx Inc. (San Jose, Calif.) this week will disclose details of the FPGA architecture that could be the first to reach 10 million gates, or 500 million transistors. The Virtex-II platform will be the basis for multiple Xilinx product families, the first parts of which are planned to begin shipping before the end of the year.

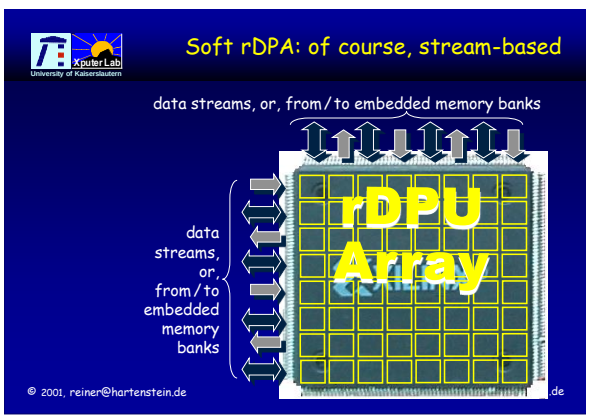
The parts are being built on 120-nm (0.12-micron) CMOS design rules and have been designed for easy migration to 100-nm processes, Xilinx officials said.

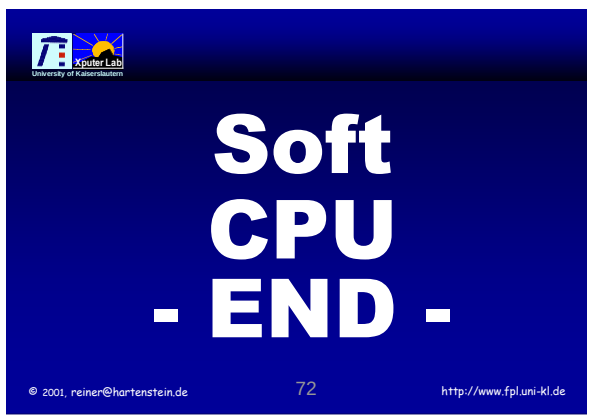
The company's largest FPGAs so far are built on the Virtex architecture, which is expected to grow to 3.2 million gates. The jump to 10 million was caused by the need for on-chip memory for larger designs, particularly in the networking and communications markets that are prime targets for larger FPGAs.

Key to Virtex-II is the release of Alliance Series 3.1i software, which brings ASIC-like features to the FPGA flow. But the Virtex-II also will include hardware changes to accommodate multiple millions of system gates.









Conclusions

- All Configware Solutions:
- New business model
- Completely new mind set
- FPGA product lifetime < 10 years
- No survival without extreme EDA fitness

Problems to be solved

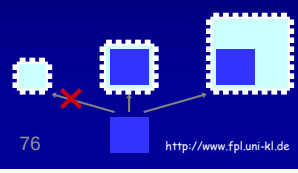
SoC Alternatives… not including C/C++ CAD Tools

- The blank sheet of paper: FPGA
- Auto design of a basic system: Tensilica
- Standardized, committee designed components*, cells, and custom IP
- Standard components including more application specific processors *, IP add-ons and custom
- One chip does it all: SMOP

*Processors, Memory, Communication & Memory Links,

Why Can't Reconfig. Software Survive?

- Resource constraints/sizes are exposed:
  - to programmer
  - in low-level representation (netlist)
- Design revolves around device size
  - Algorithmic structure
  - Exploited parallelism



Problems to be solved - END -

Reconfigurable: why?

- Exploding design cost and shrinking product life cycles of ASICs create a demand on RA usage for product longevity.
- Performance is only one part of the story. The time has come fully exploit their flexibility to support turn-around times of minutes instead of months for real time in-system debugging, profiling, verification, tuning, field-maintenance, and field-upgrades.
- A new "soft machine" paradigm and language framework is available for novel compilation techniques to cope with the new market structures transferring synthesis from vendor to customer.

RAs are heading for Mainstream

Soap Chip: System on a programmable Chip

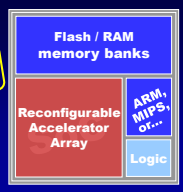
ASPP, application-specific programmable product, or,

CSoC, Configurable SoC is:
- an industry standard µProcessor,
- memory, dedicated system bus ...
- embedded reconfigurable array

RAs becoming indispensable for SoC products: a trend ...

It's a fundamental Paradigm Shift

not universal, but Domain-specific



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Schedule

time	slot
08.30 - 10.00	Reconfigurable Computing (RC)
10.00 - 10.30	coffee break
10.30 - 12.00	Compilation Techniques for RC
12.00 - 14.00	lunch break
14.00 - 15.30	Resources for Stream-based RC
15.30 - 16.00	coffee break
16.00 - 17.30	FPGAs: recent developments
17.30	end of seminar: thank you for attending

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END

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proposed scope of the course

proposed Scope :
- Data Sequencer Methodology
- Data-procedural Languages (Duality w. v. N.)
- ... supporting memory bandwidth optimization
- Soft Data Path Synthesis Algorithms
- Parallelizing Loop Transformation Methods
- Compilers supporting Soft Machines
- SW / CW Partitioning Co-Compilers
- cellular machines (Hirschbiel) - PISA
- FPGAs: recent developments

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