

To read these papers click [here](#)

1. Xputer Related Publications, Reports etc.

For more details contact Jürgen Becker, Dept. of Computer Science, University of Kaiserslautern, by e-mail no.:

abakus@informatik.uni-kl.de

- [1] Reiner W. Hartenstein, Jürgen Becker: A Two-level Co-Design Framework for data-driven Xputer-based Accelerators; to be published in Proc. of 30th Annual Hawaii Int. Conf. on System Science (HICSS-30), January 7-10, Wailea, Maui, Hawaii, USA, 1997,
- [2] Reiner W. Hartenstein, Jürgen Becker: Hardware/Software Co-Design for data-driven Xputer-based Accelerators; to be published in Proc. of 10th Int. Conf. on VLSI Design (Theme: VLSI in Multimedia Applications), January 4-7, 1997, Hyderabad, India
- [3] Reiner W. Hartenstein, Jürgen Becker, Michael Herz, Ulrich Nageldinger: A General Approach in System Design Integrating Reconfigurable Accelerators; Proc. of IEEE 1996 Int'l. Conference on Innovative Systems in Silicon; Austin, Texas, USA, October 9-11, 1996
- [4] Reiner W. Hartenstein, Jürgen Becker, Michael Herz, Rainer Kress, Ulrich Nageldinger: Co-Design and High Performance Computing: Scenes and Crisis; Proceedings of Reconfigurable Technology for Rapid Product Development & Computing, Part of SPIE's International Symposium '96, Boston, USA, Nov. 1996
- [5] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress: Custom Computing Machines vs. Hardware/Software Co-Design: from a globalized point of view; 6th International Workshop On Field Programmable Logic And Applications, FPL'96, Darmstadt, Germany, September 23-25, 1996, Lecture Notes in Computer Science, Springer Press, 1996
- [6] Reiner W. Hartenstein, Jürgen Becker, Michael Herz, Rainer Kress, Ulrich Nageldinger: A Synthesis System for Bus-based Wavefront Array Architectures; Proceedings of ASAP 96 Application Specific Array Processors, Chicago, USA, August 1996
- [7] Reiner W. Hartenstein: High-Performance Computing: Über Szenen und Krisen; GI/ITG Workshop on Custom Computing, Schloß Dagstuhl, Germany, June 1996
- [8] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress: Application Specific Microprocessors Design Methodologies: general model vs. tinker toy approach; GI/ITG Workshop on Custom Computing, Schloß Dagstuhl, Germany, June 1996
- [9] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress, Helmut Reinig: High-Performance Computing Using a Reconfigurable Accelerator; CPE Journal, Special Issue of Concurrency: Practice and Experience, John Wiley & Sons Ltd., 1996
- [10] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress: An Embedded Accelerator for Real Time Image Processing; 8th EUROMICRO Workshop on Real Time Systems, L'Aquila, Italy, June 1996
- [11] Reiner W. Hartenstein, Jürgen Becker, Michael Herz, Rainer Kress, Ulrich Nageldinger: A Parallelizing Programming Environment for Embedded Xputer-based Accelerators; High Performance Computing Symposium '96, Ottawa, Canada, June 1996
- [12] Reiner W. Hartenstein, Jürgen Becker, Michael Herz, Rainer Kress, Ulrich Nageldinger: A Partitioning Programming Environment for a Novel Parallel Architecture; 10th International Parallel Processing Symposium (IPPS), Honolulu, Hawaii, April 1996
- [13] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress: Two-Level Hardware/Software Partitioning Using CoDe-X; Int. IEEE Symp. on Engineering of Computer Based Systems (ECBS), Friedrichshafen, Germany, March 1996
- [14] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress: Two-Level Partitioning of Image Processing Algorithms for the Parallel Map-oriented Machine; 4th Int. Workshop on Hardware/Software Co-Design CODES/CASHE '96, Pittsburgh, USA, March 1996
- [15] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress, Helmut Reinig: A Novel Machine Paradigm to Accelerate Scientific Computing; Special issue on Scientific Computing of Computer Science and Informatics journal, Computer Society of India, 1996
- [16] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress: A Profiling-driven Hardware/Software Partitioning of High-level Language Specifications; IFIP Int. Workshop on Logic and Architecture Synthesis, Grenoble, France, December 1995
- [17] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress, Helmut Reinig: CoDe-X: A Novel Two-Level Hardware/Software Co-Design Framework; Proc. of VLSI Design 96 Conf., Bangalore, India, January 1996
- [18] Jürgen Becker, Reiner W. Hartenstein, Rainer Kress, Helmut Reinig: A Reconfigurable Parallel Architecture to Accelerate Scientific Computation; Proc. of Int. Conf. on High Performance Computing, New Delhi, India, December, 1995
- [19] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress, Helmut Reinig, Karin Schmidt: A Novel Hardware/Software Co-Design Framework; Journal of the Brazilian Computer Society: Special Issue on Electronic

Design Automation, no.2, vol. 2, pp. 16-26, November 1995

- [20] Reiner W. Hartenstein; Hardware/Software Co-Design; aktuelles Schlagwort; GI Informatik-Spektrum 18: p. 286-287, Springer-Verlag, Oktober 1995
- [21] Reiner W. Hartenstein; Custom Computing Machines; aktuelles Schlagwort; GI Informatik-Spektrum 18: p. 228-229, Springer-Verlag, Oktober 1995
- [22] Reiner W. Hartenstein (opening key note): Custom Computing Machines - An Overview; Workshop on Design Methodologies for Microelectronics, Smolenice Castle, Slovakia, September 1995
- [23] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress, Helmut Reinig, Karin Schmidt: A Two-Level Hardware/Software Co-Design Framework for Automatic Accelerator Generation; Workshop on Design Methodologies for Microelectronics, Smolenice Castle, Slovakia, September 1995
- [24] Reiner W. Hartenstein, Helmut Reinig: Novel Sequencer Hardware for High-Speed Signal Processing; Workshop on Design Methodologies for Microelectronics, Smolenice Castle, Slovakia, September 1995
- [25] R. W. Hartenstein, R. Kress: A Scalable, Parallel, and Reconfigurable Datapath Architecture; Sixth International Symposium on IC Technology, Systems & Applications, ISIC'95, Singapore, Sept. 6-8, 1995
- [26] R. W. Hartenstein, R. Kress: A Datapath Synthesis System for the Reconfigurable Datapath Architecture; Asia and South Pacific Design Automation Conference, ASP-DAC'95, Nippon Convention Center, Makuhari, Chiba, Japan, Aug. 29 - Sept. 1, 1995
- [27] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress, Helmut Reinig, Karin Schmidt: A Parallelizing Compilation Method for the Map-oriented Machine; Proceedings of Int. Conf. on Application Specific Array Processors, Strasbourg, France, July 1995
- [28] Jürgen Becker, Reiner W. Hartenstein, Rainer Kress, Helmut Reinig: High-Performance Computing Using a Reconfigurable Accelerator; Proceedings of Workshop on High Performance Computing, Montreal, Canada, July 1995
- [29] Reiner W. Hartenstein, Rainer Kress, Helmut Reinig: A Reconfigurable Accelerator for 32-Bit Arithmetic; International Parallel Processing Symposium, Santa Barbara, USA, April 1995
- [30] Reiner W. Hartenstein, Jürgen Becker, Rainer Kress, Helmut Reinig, Karin Schmidt: A Reconfigurable Machine for Applications in Image and Video Compression; Conference on Compression Technologies and Standards for Image and Video Compression, Amsterdam, The Netherlands, March 1995
- [31] Reiner W. Hartenstein, Karin Schmidt: Combining Structural and Procedural Programming by Parallelizing Compilation; Proceedings of the Symposium on Applied Computing, Nashville, TN, Feb. 1995
- [32] R. W. Hartenstein, R. Kress, H. Reinig: A Reconfigurable Arithmetic Datapath Architecture: GIITG-Workshop, Schloß Dagstuhl, Bericht 303, pp. 53-59, Juli 1994
- [33] R. W. Hartenstein, K. Schmidt: A Restructuring Compilation Method for the Xputer Paradigm: IWPP 94, Proceedings of the Int. Workshop on Parallel Processing, Bangalore, India, Dec. 1994
- [34] Reiner W. Hartenstein, Karin Schmidt: Parallelizing Compilation for a Novel Data-Parallel Architecture; J. P. Gray, F. Naghdy (Eds.), PCAT-94, Parallel Computing: Technology and Practice, Wollongong, Australia, pp. 126-137, Nov. 1994
- [35] A. Ast, J. Becker, R. W. Hartenstein, R. Kress, H. Reinig, K. Schmidt: Data-procedural Languages for FPL-based Machines; 4rd Int. Workshop On Field Programmable Logic And Applications, FPL'94, Prague, September 7-10, 1994, Lecture Notes in Computer Science, Springer, 1994
- [36] R. W. Hartenstein, R. Kress, H. Reinig: A New FPGA Architecture for Word-oriented Datapaths; 4th Int. Workshop On Field Programmable Logic And Applications, FPL'94, Prague, September 7-10, 1994, Lecture Notes in Computer Science, Springer, 1994
- [37] R. W. Hartenstein, R. Kress, H. Reinig: A Dynamically Reconfigurable Wavefront Array Architecture for Evaluation of Expressions; Proceedings of the Int. Conference on Application-Specific Array Processors, ASAP'94, San Francisco, IEEE Computer Society Press, Los Alamitos, CA, Aug. 1994
- [38] R. W. Hartenstein, R. Kress, H. Reinig: An FPGA Architecture for Word-Oriented Datapaths; Canadian Workshop on Field-Programmable Devices, FPD'94, Kingston, Ontario, June 13-16, 1994
- [39] R. W. Hartenstein: Hardware / Software Codesign; Internal Report No. 246/94, University of Kaiserslautern, 1994
- [40] R. W. Hartenstein, R. Kress, H. Reinig: A Reconfigurable Data-Driven ALU for Xputers; IEEE Workshop on FPGAs for Custom Computing Machines, FCCM'94, Napa, CA., April 1994
- [41] A. Ast, R. W. Hartenstein, H. Reinig, K. Schmidt, M. Weber: A General Purpose Xputer Architecture derived from DSP and Image Processing; in M. A. Bayoumi (ed.): VLSI Design Methodologies for Digital Signal Processing Architectures, Kluwer Academic Publishers, p. 365-394, 1994
- [42] A. Ast, J. Becker, R. Hartenstein, R. Kress, H. Reinig, K. Schmidt: MoPL-3: A New High Level Xputer Programming Language; 3rd Int' Workshop On Field Programmable Logic And Applications, Oxford, 7. - 10.

September 1993

- [43] A. Ast, J. Becker, R. Hartenstein, H. Reinig, K. Schmidt, M. Weber: XPUTER: ASIC or Standard Circuit?; Invited Paper: GME Fachtagung "Mikroelektronik" in Dresden 08. 10. 93, 1993
- [44] R. W. Hartenstein, H. Reinig, M. Weber: Design of an Address Generator; Proceedings 3rd Eurochip Workshop on VLSI Design Training, Grenoble, September 1992
- [45] H. Reinig: The GAG Adress Generator; (internal report), Univ. Kaiserslautern, 1992
- [46] R. Hartenstein: Avoiding Xputer Run Time Overhead by Smart Register File; (int. report), Univ. Kaiserslautern, 1992
- [47] A. Ast, R. Hartenstein, R. Kress, H. Reinig, K. Schmidt: Novel High Performance Machine Paradigms and Fast-Turnaround ASIC Design Methods: a Consequence of, and a Challenge to, Field-programmable Logic; Proceedings of the 2nd Int' Workshop on Field-Programmable Logic and Applications, 31. 08. - 02. 09. 92, Vienna Austria; Lecture Notes on Computer Science: "FPGAs, Architectures and Tools for Rapid Prototyping", Springer- Press, 1992
- [48] A. Ast, R. Hartenstein, H. Reinig, K. Schmidt, M. Weber: A Novel High-performance Machine Paradigm and ASIC Design Methodology; Int' Design Automation Workshop ("Russian Workshop"), 29. - 30. 06. 92, Moskau, 1992
- [49] R. Hartenstein, A. Hirschbiel, K. Schmidt, M. Weber: A Novel Paradigm of Parallel Computation and its Use to Implement Simple High-Performance-HW, Future Generation Computer Systems 7 91/92, p. 181-198, North Holland
- [50] R. W. Hartenstein, M. Riedmüller, K. Schmitt, M. Weber: A Novel Asic Design Approach Based on a New Machine Paradigm; Report no. 212/91, Univ. Kaiserslautern, 1991
- [51] R. W. Hartenstein, M. Riedmüller, K. Schmitt, M. Weber: A Novel Asic Design Approach Based on a New Machine Paradigm; Special Issue of IEEE Journal of Solid State Circuits on ESSCIRC'90, July 1991
- [52] R. W. Hartenstein, K. Schmidt, H. Reinig, M. Weber: A Novel Compilation Technique for a Machine Paradigm Based on Field-Programmable Logic; in Will Moore, Wayne Luk (ed.): FPGAs; Oxford 1991 International Workshop on Field Programmable Logic and Applications, Abingdon EE&CS Books, Abingdon, 1991
- [53] Reiner Hartenstein: Xputer: ein neues Maschinen-Paradigma für Höchst-leistungsrechner; Lessacher Informatik-Kolloquien, Lessach, Österreich, 18.-21. September 1990, Springer-Press, 1991 (*english: Xputer: a new Machine-Paradigm for High Performance Architectures*)
- [54] R.W. Hartenstein, H. Reinig, M. Riedmüller, K. Schmidt: A Novel Computational Paradigm: Much More Efficient Than Von Neumann Principles; 13th IMACS World Congress, Dublin Ireland, 1991
- [55] R.W. Hartenstein, A.G. Hirschbiel, M. Riedmüller, K. Schmidt, M. Weber: A High Performance Machine Paradigm Based on Auto-Sequencing Data Memory; HICSS-24, Hawaii Int' Conference on System Sciences, Koloa Hawaii, 1991
- [56] R.W. Hartenstein, A.G. Hirschbiel, M. Riedmüller, K. Schmidt, M. Weber: A Novel Paradigm of Parallel Computation and its Use to Implement Simple High Performance Hardware; Univ. Kaiserslautern, 1990
- [57] R.W. Hartenstein, A.G. Hirschbiel, M. Riedmüller, K. Schmidt, M. Weber: A Flexible Hardware Accelerator and its Applications in EDA; 16th CAVE Workshop in Gent, Belgien, 1990
- [58] R.W. Hartenstein, A.G. Hirschbiel, M. Weber: Xputers: Very High Throughput by Innovative Computing Principles; 5th Jerusalem Conference on Information Technology (JCIT), Jerusalem, Israel, Oktober 1990, Publ by IEEE Computer Society, Los Alamitos, CA, USA, 1990, p 43-50, 1990
- [59] R.W. Hartenstein, A.G. Hirschbiel, K. Lemmert, M. Riedmüller, K. Schmidt, M. Weber: Xputer Use in Image Processing and Digital Signal Processing; SPIE Visual Communication and Image Processing'90, Lausanne, Schweiz, Publ by Int Soc for Optical Engineering, Bellingham, WA, USA, p 778 -789, 1990
- [60] R.W. Hartenstein, A.G. Hirschbiel, M. Weber: A Novel Paradigm of Parallel Computation and its Use to Implement Simple High Performance Hardware; InfoJapan'90- International Conference memorating the 30th Anniversary of the Computer Society of Japan, Tokio, Japan, 1990
- [61] R.W. Hartenstein, A.G. Hirschbiel, K. Schmidt, M. Weber: A Novel ASIC Design Approach based on a New Machine Paradigm; European Solid-State Circuits Conference '90, Grenoble, Frankreich
- [62] R.W. Hartenstein, A.G. Hirschbiel, M. Riedmüller, K. Schmidt, M. Weber: Automatic Synthesis of Cheap Hardware Accelerators for Signal Processing and Image Preprocessing; 12. DAGM-Symposium Mustererkennung, Oberkochen-Aalen, 1990
- [63] R.W. Hartenstein, A.G. Hirschbiel, M. Weber: A Novel Paradigm of Parallel Computation and its Use to Implement Simple High Performance Hardware; CONPAR '90 - VAPP IV, Zürich, 1990
- [64] R.W. Hartenstein, A.G. Hirschbiel, M. Weber: The Machine Paradigm of Xputers and its Application to Digital Signal Processing Acceleration; 1990 Int' Conference on Parallel Processing, St. Charles, Illinois, 1990
- [65] R.W. Hartenstein, A.G. Hirschbiel, M. Weber: Using Xputers as Universal Accelerators for Neuro Network

- Simulation and its Applications; Int' Neural Network Conference, INNC 90, Paris, 1990
- [66] A. Ast, R.W. Hartenstein, A.G. Hirschbiel, M. Riedmüller, K. Schmidt, M.Weber: Using Xputers as Inexpensive Universal Accelerators in Digital Signal Processing; Bilkent'90 Int' Conference on New Trends in Communication, Control and Signal Processing; Ankara, Turkey, 1990
- [67] R.W. Hartenstein, A.G. Hirschbiel, M.Weber: The Machine Paradigm of Xputers and its Application to Digital Signal Processing Acceleration; Int' Workshop on Algorithms and Parallel VLSI Architectures, Pont-à-Mousson, France, 1990
- [68] R.W. Hartenstein, A.G. Hirschbiel, M.Weber: Xputers - An Open Family of Non von Neumann Architectures; Proc. of 11th ITG/GI-Conference: Architektur von Rechensystemen, VDE-Verlag, 1990
- [69] R.W. Hartenstein, A.G. Hirschbiel, M.Weber: Rekonfigurierbare ALU erlaubt Parallelisierung auf unterster Ebene; VMEbus, 1990 (*english: Reconfigurable ALU allows Parallelizing on lowest level*)
- [70] R.W. Hartenstein: Der Rechner aus dem Elfenbeinturm; Markt & Technik, Nr. 44/89, 1989 (*english: The Machine out of the Ivory-Tower*)
- [71] R.W. Hartenstein: Xputer: Xputer. Rechner nach neuartigen Prinzipien; GI Informatik Spektrum, Springer-Press, 1989 (*english: A Machine with new principles*)
- [72] R.W. Hartenstein, A.G. Hirschbiel, M.Weber: Mapping Systolic Arrays onto the Map-Oriented Machine (MoM); in: McCanny, McWhirter, Swartzlander: Systolic Array Processors, Prentice Hall, London, 1989
- [73] R.W. Hartenstein, A.G. Hirschbiel, M.Weber: A Pseudo Parallel Architecture for Systolic Algorithms; Proc. of the IFIP Workshop on Parallel Architectures on Silicon, Grenoble, 1989
- [74] R.W. Hartenstein, A.G. Hirschbiel, M.Weber: A Pseudo Parallel Architecture for Systolic Algorithms; Proc. of the Int' Conference on VLSI and CAD, Seoul (Korea), 1989
- [75] R.W. Hartenstein, A.G. Hirschbiel, M.Weber: Xputers - An Open Family of Non von Neumann Architectures; Report no. 195/89, Univ. Kaiserslautern, 1989
- [76] R.W. Hartenstein, A.G. Hirschbiel, M.Weber: MoM - a partly custom-design architecture compared to standard hardware; Compeuro 89, IEEE Press, Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA, 1989, p 5/7-9, 1989
- [77] R. Hartenstein, A. Hirschbiel, M. Weber: MOM - Map Oriented Machine; in: E. Chiricozzi & A. D'Amico: Parallel Processing and Applications, North-Holland, 1988
- [78] R.W. Hartenstein, A.G. Hirschbiel, M.Weber: "MoM - Map Oriented Machine"; Parallel Processing and Applications, North-Holland, 1988
- [79] R.W. Hartenstein, A.G. Hirschbiel, M.Weber: MoM - Map Oriented Machine, An Innovative Computing Architecture; Report,nr. 181/88, Univ. Kaiserslautern, 1988
- [80] R.W. Hartenstein, A.G. Hirschbiel, M.Weber: MoM - Map Oriented Machine; Hardware Accelerators for Electrical CAD, Adam Hilger, 1988
- [81] R. Hartenstein, A. Hirschbiel, M. Weber: A Flexible Architecture for Image Processing; Proceedings of the EUROMICRO Symposium, Portsmouth, 1987
- [82] R. Hartenstein, A. Hirschbiel, M. Weber: MOM - Map Oriented Machine; Conference on Parallel Processing and Applications, L'Aquila, Italien, 1987
- [83] R. Hartenstein, A. Hirschbiel, M. Weber: MOM - Map Oriented Machine; Proceedings of the International Workshop on Hardware Accelerators, 1987
- [84] R.W. Hartenstein, A.G. Hirschbiel, M. Weber: A Flexible Architecture for Image Processing; Microprocessing and Microprogramming, vol 21, pp 65-72, North-Holland, 1987
- [85] J. Blödel, R. Hauck, R. W. Hartenstein, M. Ryba, H. Salzmann, M. Weber: PISA: Pixel-oriented System for Layout Analysis Benutzeranleitung; Department of Computer Science & Engineering, Univ. Kaiserslautern, 1985 (*english: PISA: Pixel-oriented System for Layout Analysis User-Guidance*)
- [86] R. Hartenstein: Das E.I.S.-Verbundprojekt: Aufbruch in die Neue Mikroelektronik; Computer-Magazin, 1984 (*english: The E.I.S.-Compound-Project: Start in the New Microelectronic*)
- [87] R. Hartenstein, R. Hauck, A. Hirschbiel, W. Nebel, M. Weber: PISA, a CAD package and special hardware for pixel-oriented layout analysis; Proceedings ICCAD - Int' Conference on CAD, Sta. Clara, California, 1984
- [88] R. Hartenstein, R. Hauck, A. Hirschbiel, W. Nebel, M. Weber: PISA, a CAD package and special hardware for pixel-oriented layout analysis; Report, Univ. Kaiserslautern, 1984
- [89] P. Braun, R. Hartenstein, J. Hassdenteufel: Pixel-oriented Layout Analysis: Semi-Automatic Analyzer Generation for Design Rule Check and Circuit Extraction; Univ. Kaiserslautern, 1983
- [90] P. Braun, E. Ewald, J. Hassdenteufel, R. Hauck, A. Hirschbiel, M. Weber: DRC-KL-Programmsystem; Univ. Kaiserslautern, 1983 (*english: DRC-KL-Program-System*)